second buffer, and wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips, and wherein impedances of the second and third sections are each at least 50% greater than impedances of the first section.

2. The system of claim 1, wherein the impedances of the second and third sections are each greater than 60 ohms and the impedances of the first section are less than 40 ohms.

3. The system of claim 1, wherein the first module includes terminations for the path including the first and second sections and the first buffer is in parallel with the terminations.

4. The system of claim 3, wherein the terminations each have impedances that are at least 50% greater than the impedances of the first section.

5. The system of claim 4, wherein the impedances of the terminations are each greater than 60 ohms and the impedances of the first section are less than 40 ohms.

6. The system of claim 1, wherein the first module includes first terminations for the path including the first and second sections and the first buffer is in parallel with the first terminations, and the second module includes second terminations for the path including the first and third sections and the second buffer is in parallel with the second terminations.

7. The system of claim 1, wherein the first and second buffers each have impedances that are at least 50% greater than the impedances of the first section.

8. The system of claim 1, wherein the first buffer includes terminations for the path including the first and second sections and the second buffer includes terminations for the path including the first and third sections.

9. The system of claim 1, wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips.

10. The system of claim 9, wherein the signals include address and command signals.

11. A system comprising:

first and second modules, the first module having a first group of chips and the second module having a second group of chips;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first buffer on the first module and a second buffer on the second module;

a path including conductors in a first section that splits into a second section and third section, wherein the second section couples to the first buffer and the third section couples to the second buffer; and

wherein the first buffer includes on die terminations for the path including the first and second sections, and the second buffer includes on die terminations for the path including the first and third sections.

12. (Amended) The system of claim 11, wherein impedances of the second and third sections are each at least 50% greater than impedances of the first section.

13. The system of claim 11, wherein impedances of the second and third sections are each greater than 60 ohms and impedances of the first section are less than 40 ohms.

14. The system of claim 11, wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips.

15. The system of claim 11, wherein the signals include address and command signals.

16. A system comprising:

first and second modules, the first module having a first group of chips and the second module having a second group of chips;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first buffer on the first module and a second buffer on the second module;

a path including conductors in a first section that splits into a second section and third section, wherein the second section couples to the first buffer and the third section couples to the second buffer; and

wherein the first module includes first terminations for the path including the first and second sections and the first buffer is in parallel with the first terminations, and the second module includes second terminations for the path including the first and third sections and the second buffer is in parallel with the second terminations.

17. The system of claim 16, wherein the impedances of the second and third sections are each greater than 60 ohms and the impedances of the first section are less than 40 ohms.

18. The system of claim 16, wherein the first and second terminations each have impedances that are at least 50% greater than the impedances of the first section.

19. The system of claim 16, wherein the impedances of the first and second terminations are each greater than 60 ohms and the impedances of the first section are less than 40 ohms.

20. The system of claim 16, wherein the first module includes first terminations for the path including the first and second sections and the first buffer is in parallel with the terminations, and the second module includes second terminations for the path including the first and third sections and the second buffer is in parallel with the second terminations.

21. The system of claim 16, wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips.

22. The system of claim 16, wherein the signals include address and command signals.

23. The system of claim 16, wherein the circuit board is a printed circuit board and a motherboard.

REMARKS

Claims 1-23 are in the application of which claims 1, 11, and 16 are in independent form. Claims 1 and 12 are amended. An appendix shows amendments to the application.

Note that a supplemental Information Disclosure Statement was filed on December 12, 2002.

35 U.S.C. § 112, 2nd paragraph rejections. Claims 1-23 stand rejected under 35 U.S.C. § 112, 2nd paragraph, as being indefinite.

1. The Office action requests clarification as to the location of the first section. The first section is a section of a path that splits into second and third sections, which in turn are coupled to the first and second buffers. Merely as an example, and not a limitation, the specification (page 12, lines 26-29) states with reference to FIG. 18:

"The buffer chips buffer M1 and buffer M2 may received address and/or command signals from controller 202 on a path including conductors 204 (which has M conductors). The path splits from conductors 204 to conductors 206 and 208, with conductors 206 coupling to connector connections C25 and conductors 208 coupling to connectors connections C26."

Conductors 204, 206, and 208 are also shown in FIGS. 19 and 20.

2. The Office action requests clarification as to whether the impedances are of both the